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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,915	03/05/2002	Yoshiyuki Tonami	36856.636	6607

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,915	TONAMI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. §.133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,12 and 18-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12,18-21 and 23-26* is/are rejected.

7)☒ Claim(s) *22 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 2, 4-8, 10, 12, 18-20 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Sano (5,190,892) and Dohya (4,665,468).

Regarding claims 5, 2 and 10, AAPA teaches in figure 8 and related text a method of producing a high frequency circuit chip having a substrate 51 made of a ceramic with a high dielectric constant, a wiring pattern 52 provided on one main surface of the substrate and the wiring pattern 56 disposed on substantially all of the back main surface of the substrate 51, and a through-hole 57b Including a connecting electrode 60 for connecting the wiring pattern and the conductor layer to each other, the method comprising the steps of: Filling electrically conductive paste 60 into a perforation in the substrate, and firing the paste to form the connecting electrode of the through-hole; forming a thin film 52 with a wiring material directly on the substrate and removing the unnecessary wiring material thin film to form the wiring pattern directly on the substrate. AAPA does not teach the method of forming the wiring pattern on a mirror-polished substrate.

Sano teaches in figure 1 and related text forming a resist pattern 33 with an opening having a desired shape and size on the substrate; forming a thin film 35 with a wiring material directly on the substrate through the opening over the resist pattern after forming the resist pattern; and removing the unnecessary wiring material thin film 35 deposited on the resist pattern together with the resist pattern to form the wiring pattern 35a directly on the substrate by a lift-off method.

Dohya teaches mirror-polishing at least the surface of the fired substrate on which the wiring pattern is formed, and the fired substrate in which the through-hole having the connecting electrode is formed, before forming the wiring pattern on the mirror-polished surface (column 4, lines 52-55)..

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Sano's method of forming the wiring pattern in AAPA's device on a mirror-polished substrate, as taught by Dohya, in order to improve the electrical characteristics of the chip by providing more accurate controllable wiring pattern and by preventing damage to the substrate, and in order to prevent the undulation of the surface of the substrate, respectively. The combination is motivated by the teachings of AAPA who point out the disadvantages of using the method of forming the wiring pattern, by the teachings of Sano who points out the advantages of using a lift off method, and by the teachings of Dohya who points out the advantages of using a mirror-polished substrate (column 4, lines 45-55), respectively.

Regarding claim 4, AAPA teaches in figure 8 forming a thin-film resistor pattern 55 which is connected to the wiring pattern.

Regarding claim 6, AAPA teaches a ceramic substrate having a relative dielectric constant of at least about 10.

Regarding claims 7, 8 and 12, AAPA teaches the wiring pattern formed on at least one main surface of the substrate and the electric conductor layer formed on substantially all of the other main surface by a conductor pattern containing at least one metal selected from the group consisting of AG, Cu, and Al as a major component and having a thickness of at least about 2 microns, wherein a connecting electrode of the through-hole is formed by including at least one metal selected from the group consisting of AG, Cu, and Al as a major component.

Regarding claims 18-20 and 23-25, AAPA does not teach a thin film includes an adhesion layer, a wire bonding layer and a buffer layer. Dohya teaches a thin film includes an adhesion layer, a wire bonding layer and a buffer layer (column 6, lines21-38). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a thin film which includes an adhesion layer, a wire bonding layer and a buffer layer in AAPA's device in order to improve the reliability of the wiring structure of the device.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), Sano and Dohya, as applied to claim 5 above, and further in view of Kitamura (5,480,048).

AAPA, Sano and Dohya teach substantially the entire claimed structure, as applied to claim 5 above, except forming a protection film so as to cover the wiring pattern and cutting the substrate along desired dicing lines to obtain the high frequency circuit. Kitamura et al. teach in figure 9e forming a protection film 905 so as to cover the wiring pattern on the substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a protection film so as to cover the wiring pattern on the substrate, and to cut the substrate along desired dicing lines to obtain the high frequency circuit in AAPA's device in order to protect the wiring pattern and to obtain an operative device, respectively.

Claims 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), Sano and Dohya, as applied to claims 5 and 10 above, and further in view of JP 61091998A.

AAPA and Sano teach substantially the entire claimed structure, as applied to claims 5 and 10 above, except dipping the substrate into a rust inhibiting agent. JP 61091998A teaches dipping the substrate into a rust inhibiting agent. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to dip AAPA's substrate in a rust inhibiting agent in order to improve the quality and reliability of the substrate.

Allowable Subject Matter

Claims 22 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

The following is an examiner's statement of reasons for allowance:

Applicant Admitted Prior Art (AAPA), Sano (5,190,892) and Dohya (4,665,468) appear to be the closest prior art reference. AAPA, Sano and Dohya teach substantially the entire claimed structure, as applied to claims 5 and 10 above, except a thin film includes an adhesion layer formed on the substrate, a major conductor layer formed on the adhesion layer, a buffer layer formed on the major conductor layer, and a wire bonding layer formed on the buffer layer. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant argues that that it would not be obvious to mirror polish AAPA's device, because the undulations of the substrate 10 of Dohya are caused because substrate 10 is a multilayer substrate (the uneven combination of alumina substrates 11 and ground layers 12 cause the undulations in the multiplayer substrate 10). Unlike Dohya, AAPA and Sano only teach the use of a single layer substrate 1.

Dohya does not teach that the undulations of substrate 10 are because substrate 10 is a multilayer substrate. Dohya also does not teach that the uneven combination of alumina substrates 11 and ground layers 12 cause the undulations in the multiplayer substrate 10. Dohya states that the surfaces of the substrate are very uneven because of the state of the wire lines in the through hole, and thus it is necessary to polish the front and rear surfaces of the substrate. Therefore, it would be obvious to an artisan to mirror polish AAPA's device, as claimed. Note that it well known in the art to mirror polish a substrate, regardless whether it is a single substrate or a multiplayer substrate.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-**

1660. The Examiner is in the Office generally between the hours of 6 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
April 7, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800